IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Jeffrey Lutze et al.		
Title:	Self Aligned Non-volatile Memory Cell and Process for Fabrication		
Application No.:	10/600,259	Filing Date:	June 20, 2003
Examiner:	Not yet assigned	Group Art Unit:	2818
Docket No.:	SNDK.310US0	Conf. No.:	7482

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant(s) call(s) the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application.

☒ Copies of the documents listed on the accompanying Form PTO-1449 are enclosed.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

This information disclosure statement is submitted under 37 C.F.R. § 1.97(b) and consequently no fee should be required. The Commissioner is authorized, however, to charge any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664. This form is being submitted in duplicate.

EXPRESS MAIL NO.:

EV437667867US

Respectfully submitted,

Gerald P. Parsons — July 13, 2004
Gerald P. Parsons Date
Reg. No. 24,486

U.S. Department of Commerce, Patent and Trademark	Atty. Docket No.	Application No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	SNDK.310US0	10/600,259
	Applicant(s)	
(Use several sheets if necessary)	Jeffrey Lutze et al.	
	Filing Date	Group
	06/20/03	Unknown

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	001	6,529,410	3/2003	Han et al.			
	002	6,295,227	9/2001	Sakui et al.			
	003	5,640,032	6/17/1997	Yugo Tomioka, Tokyo (JP)			
	004	5,070,032	12/3/1991	Yuan et al.			
	005	5,923,976	7/13/1999	Kim			
	006	6,297,097	10/2/2001	Jeong			
	007	5,981,335	11/9/1999	Chi			
	008	5,343,063	8/30/1994	Yuan et al.			

U.S. Published Patent Application Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	009	U.S. 2002/0093073	7/18/2002	Mori et al.			
	010	U.S. 2004/0070021	4/15/2004	Yuan, Jack H.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	011	International Search Report, PCT/US03/32119 filed 08/10/2003
	012	U.S. Patent Application No. 09/667,344 . Yuan et al. 9/22/2000
	014	Aritome, Seiichi, "Advanced Flash Memory Technology and Trends for File Storage Application," IEDM Technical Digest, International Electronic Devices Meeting, IEEE, San Francisco, California, December 10-13. 2000, pp 33.1.1-33.1.4.
	014	Takeuchi, Y., et al., "A Self-Aligned STI Process Integration for Low Cost and Highly Reliable lGbit Flash Memories," 1998 Symposium on VLSI Technology; Digest of Technical Papers, IEEE, Honolulu, Hawaii, June 9-11, 1998, pp. 102-103.
	015	Lee, Jae-Duk, et al., "Effects of Parasitic Capacitance on NAND Flash Memory Cell Operation," Non-Volatile Semiconductor Memory Workshop, IEEE, Monterey, California, August 12-16,'2001, pp. 90-92.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	016	Hori et al., "A MOSFET with Si-implanted Gate-SiO_2 Insulator for Nonvolatile Memory Applications," IEDM 92, April 1992, pp. 469-472.
	017	Chan, et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device, " *IEEE Electron Device Letters,* Vol. EDL-8, No. 3, March 1987, pp. 93-95.
	017	Nozaki et al., "A 1-Mb EEPROM with MONOS Memory Cell for Semiconductor Disk Application," *IEEE Journal of Solid State Circuits,* Vol. 26, No. 4, April 1991, pp. 497-501.
	017	Eitan et al., "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," *IEEE Electron Device Letters,* Vol. 21, No. 11, November 2000, pp. 543-545.
	020	DiMaria et al., "Electrically-alterable read-only-memory using Si-rich $SI0_2$ injectors and a floating polycrystalline silicon storage layer," *J. Appl. Phys.* 52(7), July 1981, pp. 4825-4842.

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